AMRAD NEWSLETTER

Amateur Radio Research and Development Corporation January 1983

January 3 Meeting

Michael Kennedy of the Office of Science and Technology, FCC will be our guest speaker on Monday, January 3 at 7:30 P.M. Mike will talk about some aspects of amateur radio technology. As usual, the meeting will be at the Patrick Henry Branch Library, 101 Maple Avenue East (VA Rte 123), Vienna, Virginia. Guests are welcome.

February 7 Meeting

Bruce Brown, WA9GVK will show us the wonders of fast-scan Amateur Television.

December Meeting

We would like to thank Vic Clark, W4KFC, president of the American Radio Relay League for joining us at the December meeting. Vic had some nice words about AMRAD and filled us in on some current topics that the League is working on. These included the recent revision to the Communications Act, the ARRL's getting geared up to handle Amateur Radio license examinations and the FCC's proposal for a no-code license. On that last note, he asked for opinions of those present. He said that the group at the meeting was more amenable to a no-code license in one form or another than some other clubs that he has visited.

A few days after the meeting we received the following letter from Vic:

"A quick line to say thanks for a pleasant evening with the AMRAD club, and the chance to meet the members. I want to thank you, too, for keeping me on the mailing list for the AMRAD Newsletter, which is unique among club newsletters in its dedication to the advancement of technology in amateur radio.

"Season's Greetings to you and the members of AMRAD, and I hope that the New Year will be one of continued progress and growth."

73, Vic Clark, W4KFC

Election Results

Jeff Brennan, WB4WLW and Bill Pala, WB4NFB were reelected for two-year terms as AMRAD directors. Dick Barth, W3HWN and Dave Borden, K8MMO were reelected as alternates for one year.

Congratulations

Nancy Sanders, KB4DAJ and Barry Strassler, KA3KDF were granted their Novice licenses by the FCC. Barry is interested in getting in touch with deaf hams, possibly leading to setting up an hf net. He received a good response to a note in QST and would like to hear from other deaf hams or aspirants.

TAPR Beta TNC Boards

There is no Tucson Amateur Packet Radio column this month because everyone at TAPR (and Pete Eaton, WB9FLW from St. Louis) are busy watching Beta TNC boards come off the wave-solderering machine.

Second ARRL Packet Conference Call for Papers

The ARRL is sponsoring a second Amateur Radio Computer Networking Conference on March 19, 1983 in San Francisco, CA. The conference will be in cooperation with the 8th West Coast Computer Faire being held March 18-20.

The deadline for camera-ready papers is February 5, 1983. All papers should be mailed to Paul L. Rinaldo, W4RI, 1524 Springvale Avenue, McLean, VA 22101. If you plan to speak, please request an author's guide and advise Paul of the title of your paper immediately. Proceedings for this conference will be separate from those for the Faire which had a deadline of November 30, 1982.

Technical papers are invited on all aspects of amateur packet radio, advanced radioteletype (RTTY) including AMTOR, and related Amateur Radio digital communications via hf, vhf/uhf and satellite media. Topics may include network and system architecture, proposed standards, hardware, software, protocols, modulation and encoding schemes, and applications. This is an excellent opportunity to have your ideas influence the future of amateur digital communications.

This event will be hosted by the Amateur Radio Research and Development Corporation (AMRAD) and the Pacific Packet Radio Society (PPRS). Making up the conference committee are:

Hank Magnuski, KA6M	- Coordination (PPRS)
Stu Neblett, K6VCO	- RTTY & Packet Demos
Bob Reiling, W6JHJ	- Faire Liaison
Paul Rinaldo, W4RI	- Coordination (AMRAD) Technical Papers
Curtis Spangler, N6ECT	- West Coast Publicity

Teleconference Radio Net

We thank Bill Meyn, K4PA, for his excellent talk on AMTOR on December 2.

You are invited to listen and talk to Vic Clark, W4KFC, president of the ARRL when he discusses "The Future of Amateur Radio" on Thursday, March 3, 1983, at 8:30 EST. On Thursday, June 2, 1983, Joe Reisert, W1JR will be the featured speaker.

The following repeaters are participating:

Avon	CT	W1NI/R	224.78
Beaverton	OR	W7LJN/R	147.32
Billerica	MA	WR1ABP	147.12
Cherry Hill	NJ	WB2NQV/R	147.375
Chicago	IL	W9SRO/R	147.15
Dallas	TX	K5JD/R	146.97
Long Island	NY	WB2NHO/R	147.375
Los Angeles	CA	W6VIO/R	224.04
Madison	WI	WR9AVT/	146.76
Minneapolis	MN	WØTN/R	146.64
Phoenix	AZ	WB7AAC/R	147.36
Rochester	NY	WB2AQQ/R	145.11
Roswell	GA	N4CLA/R	145.47
San Antonio	TX	WB5FZA/R	146.70
Washington	DC	WD4IWG/R	147.21
Wichita	KS	WRØABB	146.82

The ARQ Interface Board

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Ithaca, NY 14850

This month I will briefly outline the design and functions of the interface board that I have built to perform some of the real-time tasks required in operating the W9JR FEQ ARQ System. The primary reasons for building this board were to allow the use of an 8251 USART chip to perform all parallel-to-serial data conversions, and vice versa, as well as allowing the keyboard to operate as an interrupting device. I will discuss each of the major functions on the board.

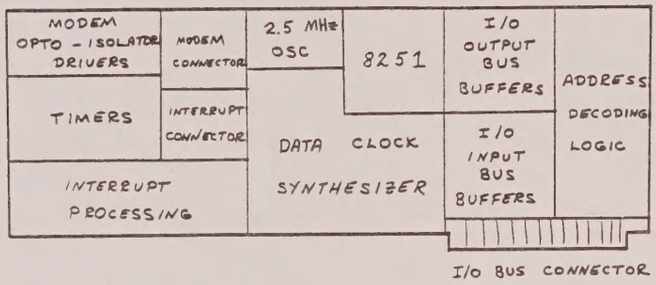

Fig. 1 - ARQ Interface Board

The board measures 4.5 by 12 inches overall, and Fig. 1 shows how the board area has been allocated. It plugs directly into the Digital Group I/O bus. Later, if others wish to use the FEC ARQ system, they will need to build a copy of this board, with slight modifications to allow direct interface to their particular I/O bus.

Address Decoding

Three chips are used to decode the four I/O port addresses needed on the board. The 8251 send and receive data registers appear at port 94H, while the 8251 control register appears at port 95H. The interrupt acknowledge logic appears at output port 96H, and a 74100 8-bit latch appears at output port 97H to control the counter chain of the data-clock synthesizer. This area of the board also handles processing of the I/O read and write signals to generate the chip-enable signals for the 8251, the 74100, and the bus buffers.

Buffers

The 8251 uses a bi-directional data bus, and this would make things very convenient when the main computer also used that architecture. As luck would have it, of course, Digital Group decided to take the inherent bi-directional bus of the Z80 and split it apart into two separate uni-directional buses. In this application, that feature forces an increase in complexity on the interface board, because it becomes necessary to combine the two I/O buses into one on the board for use by the 8251 and the other devices. Hence it was necessary to use 74125's and 7403's as input and output buffers on the board. Others duplicating this board where a bi-directional bus is already available on the motherboard can omit these and save a fair amount of space and wiring.

Data-Clock Synthesizer

A 2.5-MHz clock (a 7400 and a crystal) is provided on the board to feed both the 8251 and a synthesizer providing a programmable data clock. The synthesizer consists of a latch tied to the I/O bus and three 74193 down counters, two of which are tied to the 74100 latch outputs. The synthesizer can run the 8251 at data rates from 35 to 9600 b/s.

I originally had planned to use an 8253 programmable counter as the data clock synthesizer, but then changed my mind and used the 74193's. Having built it with the 74193's, I recommend doing it next time with the 8253. It may cost a few dollars more, but using one large chip instead of 5 small ones saves a lot of board space as well as a lot of wiring time.

Timers

While I was at it, I figured I may as well throw a couple of timers on the board just on general principles. I used an NE556 dual timer chip, and set up the RC circuit of one section to give an approximate 10-minute interval for cw i-d timing, and set the other one for 10 pulses per second, to provide a capability for some interval timing within the program itself.

The i-d timer is tied to one of the input-sensing pins of the 8251, so that its state easily can be polled at the beginning of each transmit interval to see if a cw i-d should be sent. The 10-pulse/s timer goes to a 7474 flip-flop which generates an interrupt for each pulse. The CLOCK interrupt handler then increments an 8-bit variable and a 16-bit variable for each "tick." The flip-flop is reset by an interrupt-acknowledge pulse generated in the CLOCK-handler software, to await the next pulse from the timer.

Interrupt Processing

Four different interrupts are processed by the board: the keyboard, the 10-pulse/s clock, empty XMIT buffer in the 8251, and full RCV buffer in the 8251. These are dealt with in one of two ways.

The two interrupt signals from the 8251 are fed directly to the 74148 priority encoder, where the interrupt vector is generated. (The CPU is operated in interrupt Mode 0, where we have 8 distinct interrupt vectors that can be generated, of which we are using four.) Since the 8251 is smart enough to reset its interrupt lines once the buffers are read (or written to), no acknowledge need be implemented for these two interrupts.

The keyboard and clock timer, however, both need to trigger flip-flops which generate the interrupt signals to the 74148. Then once the CPU recognizes the interrupt and jumps to the appropriate interrupt handler, an acknowledge signal is sent out to reset the flip-flop. These acknowledge signals are "trapped" off the data bus when output port 96H is addressed. Dropping one data line to TTL low resets one flip-flop, while dropping another data line resets the other.

The interrupt vector is supplied to the processor via a ribbon cable run to a DIP connnector on the CPU card.

Opto-Isolator Drivers

The ARQ Board talks to the outside world over four lines; three output and one input. Going out to the modem and radios are TX Data, XMIT/RCV, and key line signals. From the modem comes the RX Data signal. All of these lines are opto-isolated at the modem to separate the chassis ground environment of the radios and modem from that of the computer. To provide 2 mA of drive current for the isolators, 2N2222 transistors are used to drive the lines to the modem. These signals to and from the modem, as well as the key-pressed strobe from the keyboard leave the ARQ Board over another ribbon cable that connects to jacks on the back panel of the computer.

Summary

The prototype ARQ Board has been completed and tested, and it its current form performs all required functions. Some minor redesign will be required (as always) when adapting it to work with different types of computers. Importantly, however, any computer system with an 8-bit data bus, 8-bit I/O address bus, and the capability for vectored interrupts can provide the proper environment for the board.

Using the Zilog 8530 SCC

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One of the new-generation serial ICs that have come out recently is the Zilog Z8530 Serial Communications Controller (SCC). The SCC is a forty-pin device that is capable of running two separate serial channels in several different modes. It interfaces directly to a micro thru data and miscellaneous control lines, and uses only four ports or memory locations even though it has 32 write and 18 read registers internally. It has a fairly elaborate interrupt structure that is designed to work well with the Zilog Z80 processor. I have been using the chip for a couple months now on a prototype board, and it seems to be fairly easy to work with. The only problem I have had so far is that some hardware kludging is necessary to respond properly to Z80 interrupt sequences. Zilog does have this problem documented, but they don't tell you about the corrective circuitry unless you run into the problem.

Hardware Features

The SCC has two separate serial channels, each capable of going from 0 to 1M bit/second. Each channel has a programmable baud-rate generator and Digital Phase-Locked Loop (DPLL) for recovering the data clock. Each channel is also capable of running asynchronous mode with programmable data bits and all the other normal async attributes, or synchronous mode with NRZ, NRZI or FM encoding. In the sync mode almost all attributes are user programmable, including sync character and selective-address mode.

As previously mentioned, the SCC does require some external hardware to function properly with respect to Z80 interrupts. This is because the SCC is a modified version of similar peripheral designed to work on the Zilog Z-BUS. The Z-BUS responds slightly differently to interrupts and hardware resets than a Z80 does, and apparently Zilog didn't completely correct the hardware. This is true for all 8500-series peripherals. The hardware mod consists of four 74LS00-series ICs that expand the interrupt acknowledgement cycle and reset the SCC properly. Other than this timing problem, the SCC will work properly within a Z80 interrupt daisy chain and does generate interrupt vectors for the Z80.

The SCC can be programmed to be used in a Direct-Memory-Access (DMA) mode instead of using interrupts if an external DMA chip is used. In DMA mode, it generates the necessary hardware handshaking to function with a DMA controller.

The rest of the hardware interface to the CPU is thru eight data lines, a chip-select line, two address lines, and a read and write line.

Each of the two channels has serial data inputs and outputs, up to six lines for modem handshaking, and two clock input/output pins. All the lines with the exception of the clock pins are active low so they can drive TTL-to-RS-232-C devices directly.

Programming the SCC

The SCC's fifty internal registers are accessed thru only four processor ports. Each of the two serial channels has a control port and a data port. The control port is used to send commands to, and receive status from, the SCC. The data port is used to send and receive data on the serial channel. The transmit data port has a twenty-bit buffer, while the receive buffer is twenty-four bits long.

The SCC's internal control registers are accessed by first sending a pointer command to the control register telling the SCC which internal register the CPU wants to communicate with. The CPU is then capable of sending commands to, or receiving status information from, the SCC.

The CPU is capable of loading into the SCC various commands, such as:

Master Chip Reset.

Individual Channel Reset.

Master Interrupt Enable.

Many Individual Interrupt Enables.

Basic Interrupt Vector.

Async Data Configurations.

Synchronous Sync Character Register.

HDLC/SDLC Address Register.

Baud-Rate Time Constant.

Baud-Rate Clock Source.

The CPU also can read the status of the SCC thru several internal read registers. These registers contain information such as:

Resultant Interrupt Vector.

Baud-Rate Time Constant.

Interrupt Status Flags.

Interrupt Pending Flags.

Serial and Handshaking Status Flags.

As can be seen, the SCC is very interrupt oriented. It can operate in a polled enviroment (I have run it this way with good success for a while), but it works best when run using interrupts.

The SCC has a mode in which it is capable of modifying the interrupt vector by adding an offset for various interrupts. This means that the CPU doesn't have to poll the SCC after an interrupt to figure out what the SCC wants. This mode can greatly enhance interrupt speed and operation, although it will work only with a processor that accepts interrupt vectors like the Z80.

Write Register Description

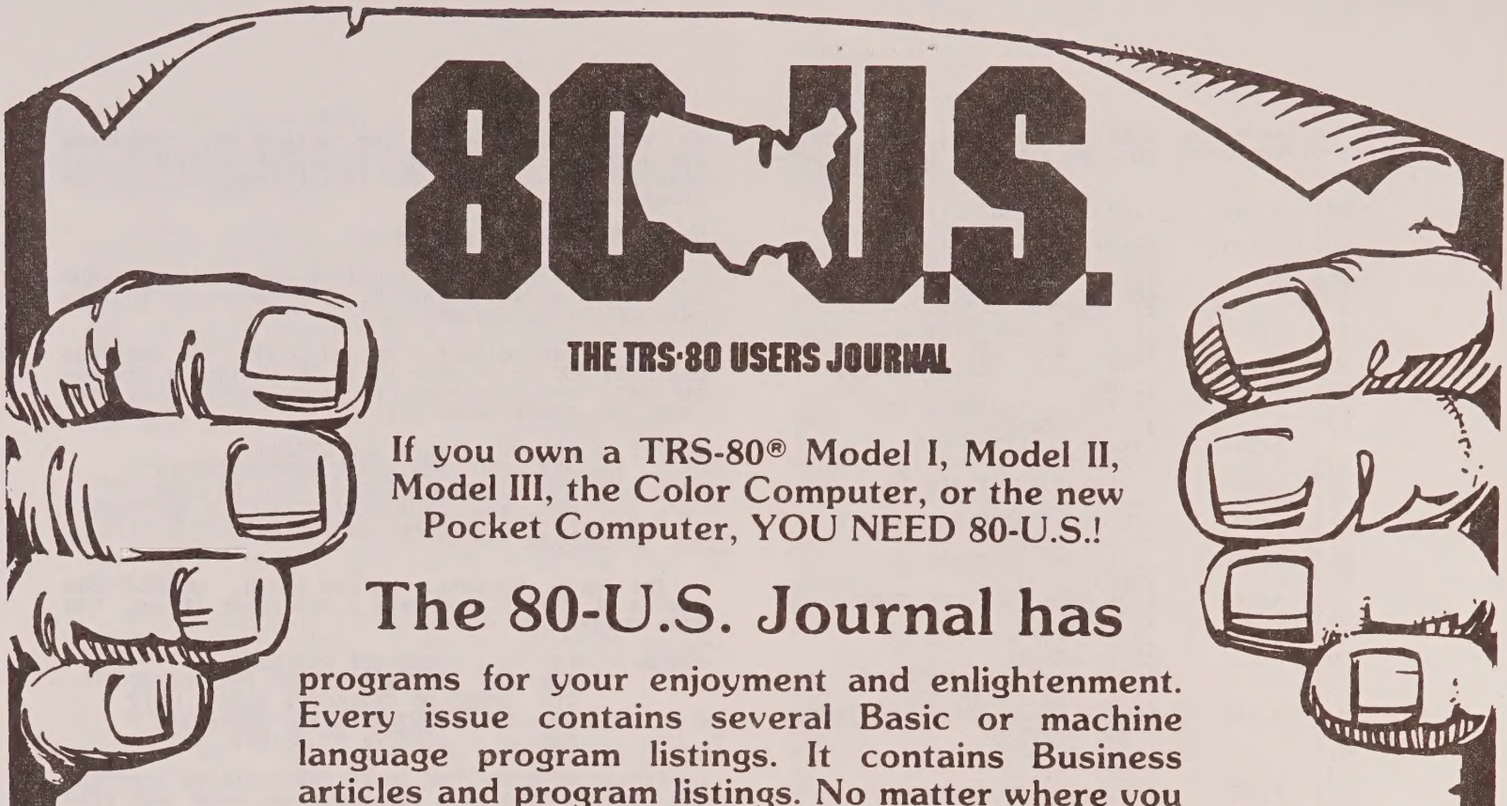
Each of the SCC serial channels (A and B) has sixteen write registers. These registers are accessed through write register 0 which is used primarily as a pointer for the other registers. Write register 0 also has some error resets and interrupt resets as it is the only register other than the data register that is directly accessible.

Write register 1 contains the main transmit and receive interrupt-enable bits, along with DMA enable and control bits.

Write register 2 contains the interrupt vector used to send back to the CPU during an interrupt acknowledgement. If the vector is to include status (which will be modified by the SCC), this will be the base address that the SCC will modify. Write register 2 is a register common to both channel A and B so it may be written to from either channel.

Write register 3 has many of the receive attributes. It has a master receive enable, SDLC/HDLC address match enable, receive CRC enable, and number of bits-per-character latches.

Write register 4 determines the clock divider (X1, X16, X32, or X64 are available), the type of sync character used in synchronous mode, the number of stop bits in asynchronous mode, and parity



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THE DEAF AND THE TTY

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Book Review: The Visicalc Book - Apple Edition

What does Visicalc have to do with the Telecommunications thrust of my monthly column? It doesn't. AMRAD received a copy of this book by Donald H. Bell. Paul Rinaldo, needing a book reviewer, and without inquiring, he handed me the book and asked me to review it. Naturally I groaned, since I have enough to do with my range of activities without being saddled with additional chores. But perhaps Paul had an ulterior motive, because the author of this book, Donald H. Bell, is from the National Technical Institute of the Deaf staff. When I browse the computer bookshelves at the popular book stores, I see this book being exhibited rather prominently for sale. So perhaps a way was found for books written by a faculty member of a school for the deaf to find its way into the regular market place.

I wish I had a copy of this book when I started to learn to use Visicalc. The original documentation, as written by Visicalc authors, Dan Bricklin and Bob Frankston, is well written. But when you try to compare Visicalc documentation by a software author with a Visicalc text book written by an educator, then there is no comparison. This is not a slur on Messrs. Bricklin and Frankston, for their efforts have revolutionized personal computing, and we are the better for it. But rather, the software people have a way of looking at things differently than educators. Or in other words, the educators simplify what the software people try to document.

Actually what I think is the winning point of this book is its twelve-page index section. I don't think anyone could find that thick an index section in proportion to the actual number of pages of text. This book has 301 pages, including twelve index pages, and to find that many pages of index could be comparable to a 600-page text of fine print. It is a joy to know that you can immediately locate a page to find out something about an obscure Visicalc feature. Under the standard documentation, one would have fits trying to locate the section on this same obscure matter. For example - if you need some clarification on what Visicalc can or cannot do with six- or seven-digit numbers, the Bell text book index will show this subject covered under page 12 and pages 127 to 136. In the regular documentation, the best you can find is under Section 4.1, under "More on Numbers and Formats," leaving you with an uneasy feeling of being undereducated on this important matter. I know because I spent a frustrating and fruitless night trying to figure out how to exhibit seven figures and to add them up without losing some decimal numbers, and not quite understanding why it does or does not work.

For all serious and dedicated Visicalc users, this book is a must on your personal shopping list, and it ranks a prominent spot next to your computer, for easy reference each time you tackle a Visicalc project and are perplexed by it.

AMRAD Amateur Radio Research and Development Corporation

Membership Application/Renewal

Mail to: Dr. William P. Pala, WB4NFB
5829 Parakeet Drive
Burke, VA 22015

See reverse for overseas mailing rates.

	Annual
Dues: Regular	$15
2nd in family same adr	8
Full-time student	5

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I agree to support the purposes of the Corporation.

Class License_____ ☐ARRL Member

Interests:
☐Packet Radio ☐Spread Spectrum
☐RTTY ☐Deaf TTY

Computer model_____
Microprocessor type_____

*Signature*_____

The Amateur Radio Research and Development Corporation (AMRAD) is a worldwide club of over 500 amateur radio and computer experimenters. It is incorporated in Virginia and is recognized by the U.S. Internal Revenue Service as a tax-exempt scientific and educational organization.

The purposes of AMRAD are to: develop skills and knowledge in radio and electronic technology; advocate design of experimental equipment and techniques; promote basic and applied research; organize technical forums and symposiums; collect and disseminate technical information; and, provide experimental repeaters.

Meetings are on the 1st Monday of each month at 7:30 P.M. at the Patrick Henry Branch Library, 101 Maple Ave E, Vienna, VA. If the first month is a holiday, an alternate date will be announced in the newsletter. Except for the annual meeting in December, meetings are normally reserved for technical talks - not business.

WD4IWG/R is an open repeater for fm voice and digital communications, especially for experimental modes. It is located at Tyson's Corner, McLean, VA. It features semi-private autopatch available to licensed members. Frequencies are: 147.81 MHz in, 147.21 MHz out. The repeater director is Jeff Brennan, WB4WLW.

WB4JFI/R is a 1200-baud half-duplex packet repeater in Falls Church, VA and may be accessed via WD4IWG/R frequencies.

WB5MMB/R is a 1200-baud simplex packet radio repeater which operates on 147.585 MHz from Vienna, VA.

The **AMRAD CBBS**, 703-734-1387, is operated by Terry Fox, WB4JFI. The system accepts 110, 300, 450 and 600-baud ASCII, Bell 103.

Handicapped Education Exchange, 301-593-7033, is operated by Dick Barth, W3HWN. HEX accepts 110/300-baud ASCII and Baudot deaf TTY/TDD calls.

AMRAD is affiliated with the American Radio Relay League (ARRL), Foundation for Amateur Radio (FAR), Northern Virginia Radio Council (NOVARC) and the Mid Atlantic Repeater Council (T-MARC).

The AMRAD Newsletter is mailed monthly to members and other clubs on an exchange basis. Technical articles, product announcements, news items, and other copy relating to amateur radio and computing are welcome. Honorariums at a rate of $15 per printed page ($20 maximum per author per issue) are paid for original material accepted. Classified ads are free to members. Commercial ad inquiries are invited. The editor reserves the right to reject or edit any portions of the copy. Items should be mailed by the 8th of the preceeding month to Paul Rinaldo, W4RI, 1524 Springvale Ave, McLean, VA 22101. Full permission for reprinting or quoting items is granted provided that credit is given to both the author and the newsletter. Mailing to U.S. and possessions is by 3rd Class bulk mail. Canadian and Mexican addresses add US$2 for postage. Overseas readers add US$8 for air mail or US$2.30 for surface.

AMRAD officers for 1982 are:

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